AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) ~~A~~ The semiconductor device ~~comprising~~ according to claim 30:

~~a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films;~~

wherein one or more wiring trenches are formed in each of said plurality of wiring insulating films along a periphery of said semiconductor chip in such a manner as to surround said circuit formation portion as said specified region,

wherein in each of said one or more wiring trenches, a conductive layer made up of copper or a copper-based conductive material is buried via a first copper diffusion preventing film, in such a manner that the respective wiring trenches corresponding to each other in said plurality of wiring insulating films are connected with each other upwardly or downwardly, and

wherein a second copper diffusion preventing film is formed between each of said plurality of wiring insulating films and an other one of said plurality of wiring insulating films being adjacent thereto upwardly or downwardly, in such a manner as to be connected with the corresponding first copper diffusion preventing film.

2. (Currently Amended) The semiconductor device according to claim ~~1~~ 30, wherein said at least one conductive layer is connected to a diffusion region formed in said semiconductor substrate.

3. (Currently Amended) The semiconductor device according to claim ~~1~~ 30, wherein at least one of said plurality of wiring insulating films comprises a low-dielectric constant film.

4. (Currently Amended) ~~A~~ The semiconductor device ~~comprising~~ according to claim 34:

~~a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,~~

wherein at least one seal ring made of a conductive material is formed along a periphery of said semiconductor chip so as to surround said circuit formation portion as said specified region, said at least one seal ring being connected with said semiconductor substrate and being buried in said plurality of wiring insulating films in such a manner as to extend over said wiring insulating films.

5. (Currently Amended) ~~A~~ The semiconductor device ~~comprising~~ according to claim 34:

~~a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor~~

~~substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films;~~

~~wherein a plurality of seal rings each made of a conductive material is formed along a periphery of said semiconductor chip so as to surround said circuit formation portion, said seal ring beings connected with said semiconductor substrate and being buried in said plurality of wiring insulating films in such a manner as to extend over said wiring insulating films, and~~

wherein one or more slit-like notches are formed at specified positions in said ~~plurality of~~ seal rings in such a manner that the respective slit-like notches in two seal rings being adjacent to each other are not aligned.

6. (Currently Amended) The semiconductor device according to claim ~~4~~ 34, wherein, said at least one seal ring comprises a damascene wiring structure as well as said multi-layer interconnection of said circuit formation portion.

7. (Original) The semiconductor device according to claim 6, wherein said damascene wiring structure comprises a single damascene wiring structure.

8. (Original) The semiconductor device according to claim 6, wherein said damascene wiring structure comprises a dual damascene wiring structure.

9. (Original) The semiconductor device according to claim 6, wherein said damascene wiring structure comprises a combination of a single damascene wiring structure and a dual damascene wiring structure.

10. (Currently Amended) The semiconductor device according to claim ~~4~~ 34, wherein said at least one seal ring is connected to a diffusion region formed in said semiconductor substrate.

11. (Currently Amended) The semiconductor device according to claim ~~4~~ 34, wherein said at least one seal ring is connected via a contact to a diffusion region formed in said semiconductor substrate, said contact and said diffusion region being formed so as to match approximately said at least one seal ring in shape.

12. (Currently Amended) The semiconductor device according to claim ~~4~~ 34, wherein said at least one seal ring is connected via a contact to a diffusion region formed in said semiconductor substrate, said contact and said diffusion region being formed without matching said at least one seal ring.

13. (Currently Amended) The semiconductor device according to claim ~~4~~ 34, wherein said at least one seal ring comprises copper or a copper-based conductive material.

14. (Currently Amended) The semiconductor device according to claim ~~4~~ 34, wherein at least one of said plurality of wiring insulating films comprises a low-dielectric constant film.

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Currently Amended) ~~A~~ The semiconductor device ~~comprising~~ according to claim 34:

~~a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,~~

wherein an assembly pad, a characteristics evaluation pad, or a screening evaluation pad ~~each are~~ is formed on a surface of said semiconductor substrate in such a manner to be electrically connected to said circuit formation portion, and

wherein at least one seal ring made of a conductive material is formed in such a manner as to surround said assembly pad, said characteristics evaluation pad, or said screening evaluation pad as said specified region, said at least one seal ring being connected with said semiconductor substrate and extending over said wiring insulating films.

23. (Original) The semiconductor device according to claim 22, wherein, at least one bottomed seal ring, being not connected with said semiconductor substrate, is formed in such a manner as to surround said assembly pad, said characteristics evaluation pad, or said screening evaluation pad.

24. (Original) The semiconductor device according to claim 22, wherein said at least one seal ring comprises a damascene wiring structure.

25. (Original) The semiconductor device according to claim 23, wherein said at least one bottomed seal ring comprising a damascene wiring structure.

26. (Currently Amended) ~~A~~ The semiconductor device ~~comprising~~ according to claim 34:

~~a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,~~

wherein a plurality of fuse elements for each replacing a defective circuit element therewith is provided on a surface of said semiconductor substrate in such a manner as to be electrically connected with said circuit formation portion, and

wherein at least one seal ring each made of a conductive layer is formed in such a manner as to surround said plurality of fuse elements as said specified region, said at least one seal ring being connected with said semiconductor substrate and extending over said plurality of wiring insulating films.

27. (Original) The semiconductor device according to claim 26, wherein, at least one bottomed seal ring, being not connected with said semiconductor substrate, is formed in such a manner as to surround said plurality of fuse elements

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28. (Original) The semiconductor device according to claim 26, wherein said at least one seal ring comprises a damascene wiring structure.

29. (Original) The semiconductor device according to claim 27, wherein said at least one bottomed seal ring comprises a damascene wiring structure.

Please add the following new claims:

30. (New) A semiconductor device comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein one or more wiring trenches are formed in each of said plurality of wiring insulating films along a periphery of said semiconductor chip in such a manner as to surround a specified region on said semiconductor substrate,

wherein in each of said one or more wiring trenches, a conductive layer made up of copper or a copper-based conductive material is buried via a first copper diffusion preventing

film, in such a manner that the respective wiring trenches corresponding to each other in said plurality of wiring insulating films are connected with each other upwardly or downwardly, and

wherein a second copper diffusion preventing film is formed between each of said plurality of wiring insulating films and another one of said plurality of wiring insulating films being adjacent thereto upwardly or downwardly, in such a manner as to be connected with the corresponding first copper diffusion preventing film.

31. (New) The semiconductor device according to claim 30,

wherein an assembly pad, a characteristics evaluation pad, or a screening evaluation pad is formed on a surface of said semiconductor substrate in such a manner to be electrically connected to said circuit formation portion, and

wherein one or more wiring trenches are formed in each of said plurality of wiring insulating films along a periphery of said semiconductor chip in such a manner as to surround said assembly pad, said characteristics evaluation pad, or said screening evaluation pad as said specified region.

32. (New) The semiconductor device according to claim 30,

wherein a plurality of fuse elements for each replacing a defective circuit element therewith is provided on a surface of said semiconductor substrate in such a manner as to be electrically connected with said circuit formation portion, and

wherein one or more wiring trenches are formed in each of said plurality of wiring insulating films along a periphery of said semiconductor chip in such a manner as to surround said plurality of fuse elements as said specified region.

33. (New) The semiconductor device according to claim 30,

wherein one or more slit-like notches are formed at specified positions in said conductive layer in such a manner that the respective slit-like notches in two said conductive layers being adjacent to each other are not aligned.

34. (New) A semiconductor device comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein at least one seal ring made of a conductive material is formed along a periphery of said semiconductor chip so as to surround a specified region on said semiconductor substrate, said at least one seal ring being connected with said semiconductor substrate and being buried in said plurality of wiring insulating films in such a manner as to extend over said wiring insulating films.